Experiment No. 03

**Layout of CMOS inverter**

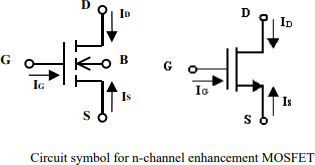
**OBJECTIVE:** To simulate the Layout of the CMOS inverter.

**SOFTWARE**: Electric VLSI , LT Spice

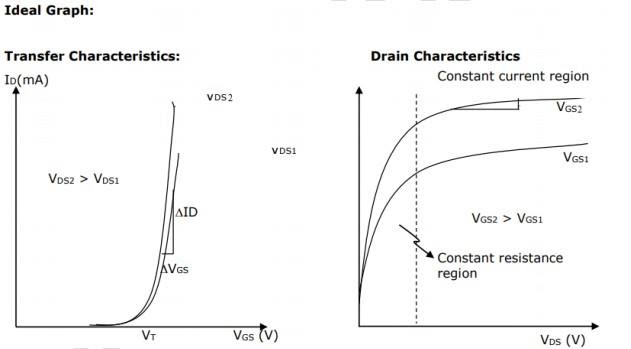
**THEORY:** The MOSFET is actually a four-terminal device, whose substrate, or body terminal must be always held at one of the extreme voltage in the circuit, either the most positive for the PMOS or the most negative for the NMOS. One unique property of the MOSFET is that the gate draws no measurable current (IG=0).

Current flow between the source and drain terminals is controlled by the voltage VGS applied between the gate and source terminals. If the gate-to-source voltage VGS < VT no current can flow between the source and the drain – i.e. the transistor is OFF; if VGS > VT, then current can flow between the source and the drain

– i.e. the transistor is ON. The circuit symbol for an n-channel enhancement-mode (VT > 0 Volts) MOSFET is shown in Figure, along with the terminal current reference directions.



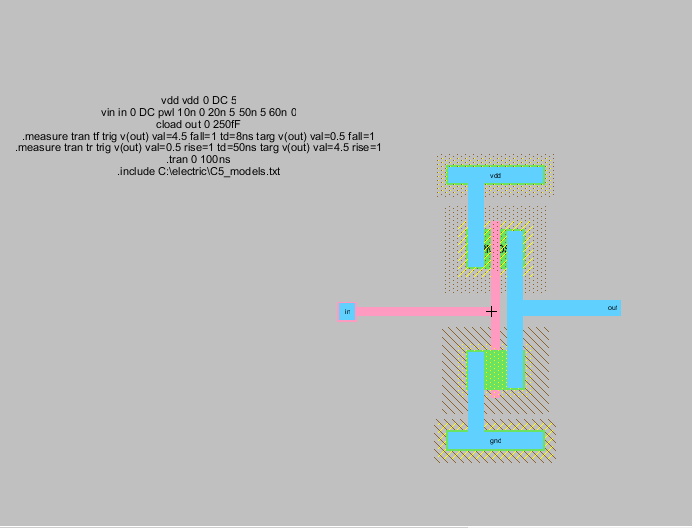
In the ON state, the current IDS flowing from the drain to the source will depend on the potential difference VDS between the drain and the source: IDS increases with increasing drain-to-source voltage VDS as long as the drain voltage is at least  VT below the gate voltage, i.e. as long as (VGS- VT) > VDS. When VDS increases above (VGS- VT), IDS saturates at a constant value. V-I operating curves for a typical n-channel enhancement-mode Field Effect Transistor (FET). As can be seen in the figure, for each value of VGS there is a unique curve of IDS Vs VDS**.**

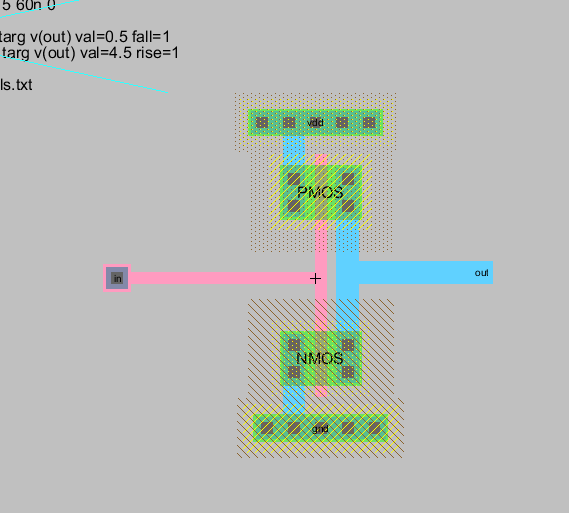


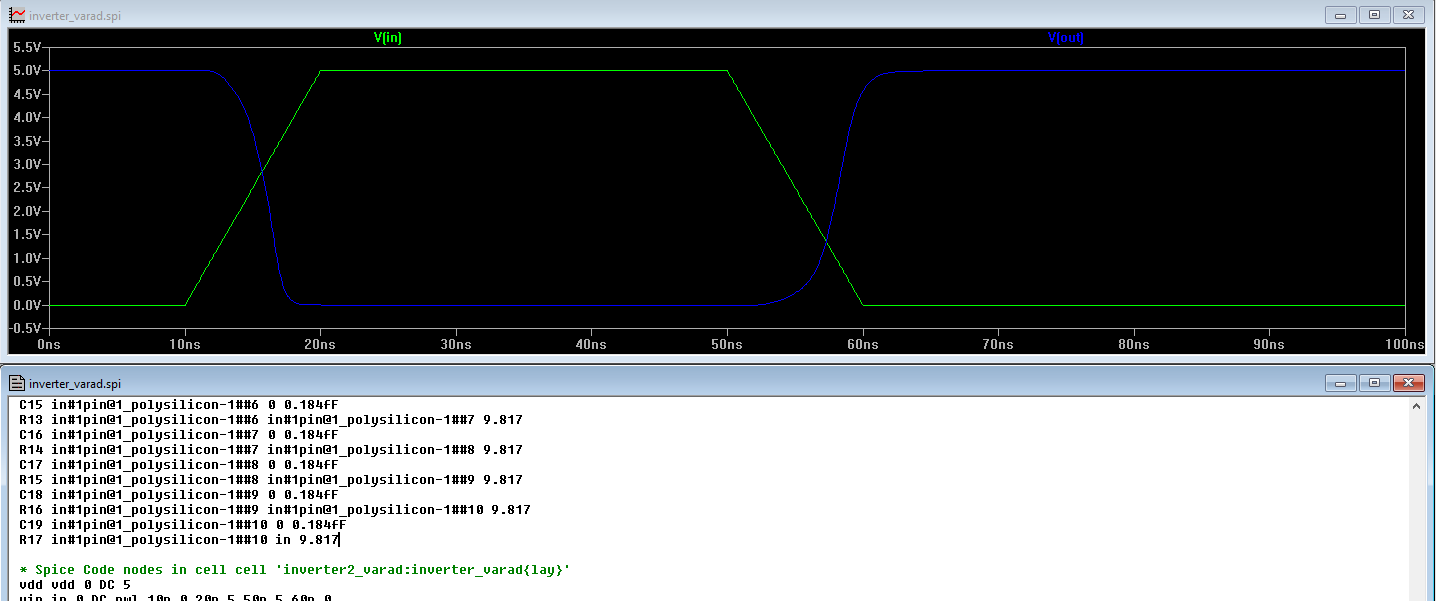
**PROCEDURE:**

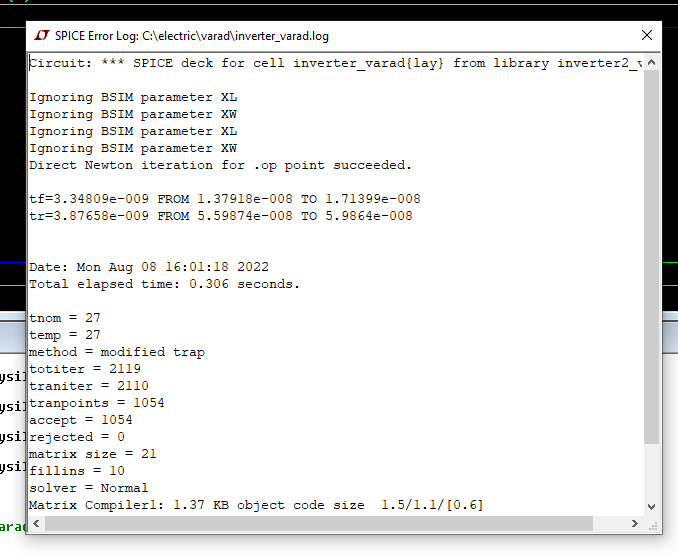
1. Open Electric VLSI.
2. In **Files** Menu---click on **new library**---Give name to library.
3. In **Edit** Menu---click on **New Cell**---give name to cell---Select view as –**Layout**.
4. Go to **Components**---Select each required component----do connections.
5. In **Tools** menu---go to **Simulation(spice)**---**Set Spice model**. Select text Spice model and edit it to PMOS or NMOS according to the device.
6. **Create export**s as—in and out.
7. Write Spice code---by clicking on **Misc** in **Components** and click on **spice code**.
8. Save library.
9. Simulate the layout --- in **Tools** menu ----go to **Simulation(spice)**--- click on **Write Spice deck**.
10. LT Spice window gets opened. There Right click on the black window---click on **add trace**.
11. To see fall and rise time--- in **Edit** menu ---click on **SPICE error log**.

**OUTPUT:**









**CONCLUSION:**

**Designing and Simulation of the layout of the CMOS transistor in electric vlsi was performed successfully. The propagation delay of cmos was plotted in ltspice. The delay is shown is spice error log.**